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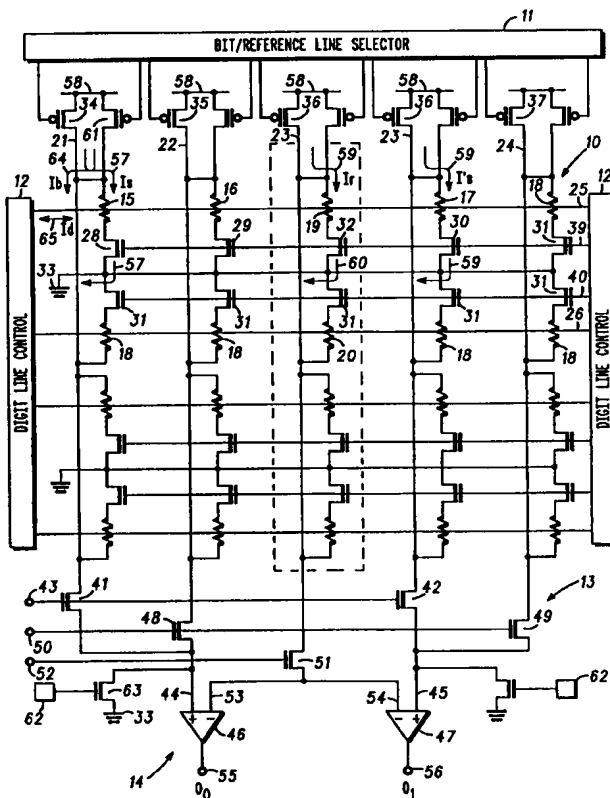
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(54) Title: MRAM ARRAY HAVING A PLURALITY OF MEMORY BANKS

(57) Abstract

An MRAM device has a new type of memory bank (10) that includes bit lines (21-24), a reference line (27) and digit lines (25, 26), on intersections of bit lines and digit lines a plurality of magnetic memory cells (15-18) are arrayed. Bit lines are formed on both sides of the reference line on a substrate. Since each bit line is fabricated closely to the reference line, each cell has substantially the same hysteresis characteristics, which allow the MRAM device to provide a steady operation mode.



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INTERNATIONAL SEARCH REPORT

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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 173 873 A (WU JIIN-CHUAN ET AL) 22 December 1992 (1992-12-22) column 5, line 23 -column 6, line 44; figures 4,5	1,2,4,5 3,6-10
A	----	
X	EP 0 613 148 A (IBM) 31 August 1994 (1994-08-31) column 4, line 43 -column 5, line 23; figure 3	1-4

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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EP 0613148 A	31-08-1994	US 5343422 A	30-08-1994
		JP 2784439 B	06-08-1998
		JP 6295419 A	21-10-1994

MRAM ARRAY HAVING A PLURALITY OF MEMORY BANKS

Field of the Invention

5 The present invention relates to a magnetic random access memory, and more particularly, to a magnetic random access memory with a plurality of memory banks, each memory bank having bit lines allocated on both sides of a reference line.

10

Background of the Invention

15 A magnetoresistive random access memory (MRAM), which is one of non-volatile memory devices, includes a plurality of magnetic memory cells. It is known that the magnetoresistive effect appears in multi-layer films that are alternately stacked by magnetic layers and non-magnetic layers. Magnetic resistance over a magnetic memory cell indicates minimum and maximum values when magnetization vectors in magnetic layers point in the same or opposite directions, respectively. The same and opposite directions of magnetization vectors in two magnetic layers are called "Parallel" and "Anti-parallel" states, respectively. When magnetic material is employed for a memory device, Parallel and Anti-parallel directions, for example, are logically defined as "0" and "1" states, respectively. The magnetization vectors in magnetic layers are very quickly switched to another direction by an application of a magnetic field over a switching point, and maintain the magnetization direction even without a magnetic field.

30

 The MRAM device normally has magnetic memory cells arranged on intersections of metal lines, which are placed in rows and columns. The MRAM circuit, for instance, is described in a co-pending U.S. patent application entitled

"MAGNETORESISTIVE RANDOM ACCESS MEMORY WITH SHARED WORD AND DIGIT LINES," Motorola docket No. CR98-038, filed July , 1998 assigned to the same assignee, and incorporated herein by reference.

5 The MRAM device generally is formed on a substrate such as a semiconductor or glass. Magnetic and non-magnetic layers are sequentially deposited on the substrate and etched down to form magnetic memory cells, which are 0.2 μm by 0.3 μm in size, for instance. The magnetic layer usually
10 has a 10-100Å thickness while the non-magnetic layer is 10-30Å thick. The thickness of the magnetic and non-magnetic layers are deposited on the substrate as invariably and evenly as possible, which allows each magnetic memory cell on the substrate to provide steady and constant hysteresis
15 characteristics. It, in reality, is very hard to control and keep a thickness of each layer constant to every magnetic memory cell on the entire substrate.

 The MRAM device includes magnetic memory cells for storing specific information, and reference magnetic memory
20 cells where a reference state is maintained. In order to read states stored in a magnetic memory cell (active or target cell), a sense current and a reference current are applied to the target cell and a reference magnetic memory cell (reference cell), respectively. The target and
25 reference cells generate voltage drops across the cells that correspond to magnetic resistance values of the target and reference cells, respectively. These voltages are compared to each other to determine states in the target cell. Therefore, it is desirable that each magnetic cell has as
30 same or similar hysteresis characteristics as possible, in order to execute a steady reading process and to get states correctly.

 Accordingly, it is a purpose of the present invention to provide an improved MRAM device that has a high-speed,

high-density, and low power memory.

It is another purpose of the present invention to provide an improved MRAM device that has a high reliability reading process.

- 5 It is still another purpose of the present invention to provide an improved MRAM device that has a high tolerance for temperature variation.

Summary of the Invention

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- These needs and others are substantially met through provision of a magnetoresistive random access memory (MRAM) device that includes memory banks, each memory bank having a reference line, bit lines and digit lines. Bit lines are allocated parallel to the reference line and on both sides of the reference line. Word lines and digit lines, which are perpendicular to bit lines, form intersections on which magnetic memory cells are arrayed for storing information. Reference magnetic memory cells are arranged on intersections of the reference line and digit lines. A memory cell has magnetic layers separated by a non-magnetic layer. Magnetic and non-magnetic layers, for example, are deposited on a substrate with thicknesses of 10-100Å and 10-30Å, respectively. The difficulty for uniformly forming the thickness and the size of the memory element over the entire substrate allows memory cells to indicate different hysteresis characteristics that result in a reading error. In order to prevent mistakenly reading states in a magnetic memory cell, the present invention divides a memory array into a plurality of memory banks. Each memory bank includes a reference line, and bit lines that are formed on both sides of the reference line. Since bit lines are formed adjacent to the reference line on the substrate, magnetic memory cells have the same or similar hysteresis
- 15
20
25
30

characteristics as reference memory cells.

Brief Description of the Drawings

5 FIG. 1 shows a memory bank circuit and other peripheral circuits in an MRAM device;

 FIG. 2 shows a simplified and enlarged magnetic memory cell with magnetic layers separated by a non-magnetic layer;

10 FIG. 3 shows a graph illustrating hysteresis characteristics of the magnetic memory cell described in FIG. 2;

 FIG. 4 shows another embodiment for an MRAM element circuit; and

15 FIG. 5 shows an entire MRAM device circuit having four memory banks.

Detailed Description of the Preferred Embodiments

20 FIG. 1 shows a memory bank circuit 10 and other peripheral circuits including a bit/reference line selector 11, a digit line control 12, a selector 13, and a comparator circuit 14. These circuits are fabricated on a semiconductor or a glass substrate. Although one memory bank is illustrated in FIG. 1, it should be understood that
25 an MRAM device includes a plurality of memory banks for more memory capacity, which will be described hereinafter with reference to FIG. 5.

 Memory bank 10 has magnetic memory cells (memory cells) 15-18 and reference memory cells 19 and 20. Memory cells
30 15-18 are placed on intersections of sense or bit lines 21-24 and torque or digit lines 25 and 26 perpendicular to bit lines 21-24, while reference memory cells (reference cells) 19 and 20 are placed on intersections of a reference line 27 and digit lines 25 and 26. Memory cells 15-18 and reference

cells 19 and 20 form the same cell structure as illustrated in FIG. 3, the details of which will be discussed hereinafter. Memory cells 15-18 and reference cell 19 are coupled in series to transistors 28-32, which control a
5 current flow in memory cells 15-18 and reference cell 19 to a ground or common line 33. As can be seen in FIG. 1, memory bank 10 has a single reference line and four bit lines. Every two lines of four bit lines are symmetrically allocated on both sides of the reference line, thereby each
10 memory cell on bit and reference lines is closely placed on the substrate. Although memory bank 10 includes two bit lines on both sides of the reference line, furthermore it is possible to add other bit lines for enlargement of the memory capacity.

15 Bit lines 21-24 and reference line 27 are coupled to switching transistors 34-38 that selector 11 manages so as to provide a sense current and a reference current, respectively. Digit line control 12 places digit lines 25 and 26 adjacent the memory cells, and couples lines 39-40 to
20 transistors 28-32. Transistors 41 and 42, in response to a signal on terminal 43, couple bit lines 21 and 23 to non-inverting inputs 44 and 45 of comparators 46 and 47, while transistors 48 and 49, in response to a signal on terminal
25 50, couple bit lines 22 and 24 to non-inverting inputs 44 and 45 of comparators 46 and 47 as well. Transistor 51 controlled by a signal on a terminal 52 couples reference line 27 to inverting inputs 53 and 54 of comparators 46 and
30 47. Comparators 46 and 47 compare voltages on non-inverting inputs 44 and 45 to reference voltage on inverting inputs 53 and 54 to produce output signals O_0 and O_1 on output terminals 55 and 56.

In an operation for reading states in target cells 15 and 17, for example, selector 11 sends turn-on signals to gate electrodes of transistors 34 and 36 and transistor 38

to activate bit lines 21 and 23 and reference line 27, respectively. Next, line control 12 provides a turn-on signal on line 39 to allow transistors 28-32 to turn on. Consequently, a sense current I_s , indicated by an arrow 57, flows from a power line 58 through transistor 34, target cell 15 and transistor 28 to common line 33 while a sense current I_s' , indicated by an arrow 59, flows from power line 58 through transistor 36, target cell 17 and transistor 30 to common line 33. As well as sense currents I_s and I_s' , a reference current I_r expressed by an arrow 60 is supplied from power line 58 through transistor 38, reference cell 19 and transistor 32 to common line 33. Sense currents I_s and I_s' generate voltage drops across target cells 15 and 17 that are introduced to non-inverting inputs 44 and 45 of comparators 46 and 47 after turning transistors 41 and 42 on. Furthermore, reference current I_r produces a voltage drop across reference cell 19 that is conducted through transistor 51 to both inverting inputs 53 and 54 of comparators 46 and 47. Comparators 46 and 47 compare voltage values on non-inverting and inverting inputs. Comparator 46, for instance, provides a high-voltage signal on output terminal 55 when the voltage drop across target cell 15 is higher than the reference cell 19; otherwise a low-voltage appears on output terminal 55.

A gate voltage applied to transistor 38 from line selector 11 controls reference current I_r . Assuming a magnetic memory cell produces a maximum voltage V_{max} at an Anti-parallel state and a minimum voltage V_{min} at a Parallel state, reference current I_r adjusts a reference voltage V_{ref} generated across a reference magnetic cell so as to have a half voltage between V_{max} and V_{min} ; that is,

$$V_{ref} = (V_{max} + V_{min})/2$$

In order to write states in target cell 15, for instance, line selector 11 turns on transistor 61 and a turn-on signal is provided on terminal 43 to turn transistor 41 on, which allows bit line 21 to activate. At the same time a bit line program control 62 turns on transistor 63. Then bit current I_b indicated by an arrow 64 flows from power line 58 through transistor 61, bit line 21, transistor 41, and transistor 63, to common line 33. Furthermore, line control 12 activates digit line 25 to provide digit current I_d indicated by an arrow 65. Bit current I_b and digit current I_d generate magnetic fields, respectively. These magnetic fields are combined toward target cell 15. The combination of the magnetic fields from I_b and I_d is sufficient to switch the magnetization vectors in target cell 15, however regarding other cells 16-18, the individual magnetic fields are less than the magnetic field required to change the magnetization direction in a memory cell. At least one of the bit current or the digit current has to be reversible to store the two different states in the selected target cell. In this embodiment, digit line control 12 manages the directions of digit current I_d . During a program mode, digit line control 12 pulls down lines 39 and 40, turning off transistors 28-32. Also comparators 46 and 47 are disabled, and no current flows through reference line 23 during a program mode.

FIGS. 2 and 3 show an isometric view of a simplified and enlarged memory cell structure 70 and hysteresis characteristics 75 of memory cell 70 in FIG. 2. It should be noted that other types of magnetic memory cells can be employed for the memory device. Memory cell 70 has three layers that include first and second magnetic layers 71 and 72 separated by a non-magnetic layer 73. First and second magnetic layers 71 and 72 use magnetic material such as CoFe and NiFeCo , respectively. Magnetization vectors in first

magnetic layer 71, for example, are magnetically pinned by an antiferromagnetic layer (not shown) that is placed adjacent layer 71. Second magnetic layer 72, which is magnetically free, alternates magnetization vectors
5 responding to an external magnetic field. Non-magnetic layer 73, for example, is formed by an insulating material such as Al_2O_3 and has a thickness of around 30\AA . The thin thickness allows non-magnetic layer 73 to form a tunneling junction between first and second magnetic layers 71 and 72,
10 through which a tunneling current flows. As will be seen in FIG. 3, a magnetic resistance of the memory cell changes according to directions of magnetization in second magnetic layer 72 that causes a tunneling current in non-magnetic layer 73 to vary. The magnetic layers would be patterned to
15 substantially align the magnetization as shown in U.S. Patent No. 5,757,695.

Referring to FIG. 3 again, the abscissa of FIG. 3 indicates a direction and strength of a magnetic field applied to memory cell 70. The ordinate represents the
20 magnetic resistance of the memory cell 70. Assuming memory cell 70 is in the state that magnetization vectors in layers 71 and 72 point in the Parallel state (same direction) under no external magnetic field, the external magnetic field changes to a value H_1 moving to the right along the
25 abscissa. As shown by curve 76, magnetization vectors in second magnetic (free) layer 72 are switched to the left at a magnetic field H_1 and magnetization vectors in layers 71 and 72 are oriented in the Anti-parallel state (opposite direction) as indicated by arrows 77. Consequently, a
30 magnetic resistance of memory cell 70 increases from R by ΔR . Next changing the magnetic field from H_1 as shown by curve 78, magnetization vectors in second magnetic layer 72 are switched at a magnetic field H_2 to the right. Consequently the magnetic resistance is lowered to R by ΔR

and magnetization vectors in layers 71 and 72 point in the Parallel direction as indicated by arrows 79. An example of the memory cell structure is shown in U.S. Patent No. 5,768,181.

5 Turning now to FIG. 4, another embodiment of an array 80 of cells similar to cell 70 in FIG. 2 is illustrated with the cells being oriented in rows and columns. Only four cells 81 through 84 are illustrated for convenience, but it will be understood that any desired number of cells which
10 can be practically fabricated can be employed. A plurality of diodes 85 through 88 are supplied, one each being associated with each cell 81 through 84. In this embodiment, one terminal of the associated diode is connected to the lower or upper magnetic layer of the
15 associated cell by means of an electrically conductive portion, which may include material such as a conductive layer, or solder, or the diodes may be integrated into a substrate or upper layer and formed with the conductive portion as a portion of the diode. A second terminal of the
20 diode is connected to a sense line and the other of the first and second magnetic layers of the cell are connected to a word line as shown in U.S. Patent No. 5,734,605.

In FIG. 4, cell 81 has a magnetic layer connected to one terminal of diode 85 and the other magnetic layer
25 connected to a bit line B_0 . The second terminal of diode 85 is connected to a word line W_0 . Thus, cell 81 is uniquely addressed by selecting bit line B_0 and word line W_0 . Any change in resistance of cell 81 can be easily and quickly sensed by connecting sensing apparatus between bit line B_0
30 and word line W_0 . To select cell 81, diode 85 is forward biased. Once diode 85 is forward biased, current flows from bit line B_0 through cell 81 and diode 85 to word line W_0 . All other diodes 86-88 are reverse biased. As a result, no current flows through cell 82-84.

FIG. 5 shows an entire MRAM circuit 90 that includes memory banks 91-94, a bit/reference line control 95, digit line control 96, selector 97, and a comparator circuit 98. These circuits are fabricated on a semiconductor or a glass substrate. MRAM circuit 90 has four memory banks 91-94. It should be noted that more memory banks are established upon request of more memory capacity. Only memory bank 91 will be discussed hereinafter because memory banks 92-94 have the same circuit structure and operation as memory bank 91.

Memory bank 91 includes one reference line R.LINE0, and one hundred twenty eight bit lines B.LINE0-B.LINE127 that are divided into four groups, that is, first group for bit lines B.LINE0-B.LINE31, second group for bit lines B.LINE32-B.LINE63, third group for bit lines B.LINE64-B.LINE95, and fourth group for bit lines B.LINE96-B.LINE127. First and second groups and third and fourth groups are symmetrically and physically allocated on both sides of reference line R.LINE0 on a substrate. Magnetic memory cells are arrayed on intersections of bit lines B.LINE0-B.LINE127 and digit lines D.LINE0-D.LINE N while reference magnetic memory cells are placed on intersections of reference line R.LINE0 and digit lines D.LINE0-D.LINE N. Each memory cell, for instance, a cell 101 is coupled to a transistor 105 that, in response to a signal on a word line W.LINE0, switches on and off a sense current supplied from bit line B.LINE0 to cell 101. As mentioned earlier in conjunction with FIG. 4, transistor 105 is replaceable with a diode.

In a reading operation mode, one bit line in each group is selected and activated to read magnetic states in a target cell. For example, when line control 95 selects bit lines B.LINE0 in the first group, B.LINE32 in the second group, B.LINE64 in the third group, and B.LINE96 in the fourth group, and at the same time line control 96 sends a turn-on signal on word line W.LINE0. Then, target cells

101-104 are activated to provide sense currents therein, respectively. At the same time of activation for the bit lines, line control 95 supplies a reference current into reference line R.LINE0 to generate a reference voltage
5 across a reference memory cell 106. Voltage drops across target cells 101-104 and the reference voltage are applied to comparators 111-114 through selector 97. A voltage drop across target cell 101, for example, is introduced to selector 97 by way of bit line B.LINE0, while the reference
10 voltage is provided to selector 97 through reference line R.LINE0. Selector 97 connects bit line B.LINE0 and reference line R.LINE0 to non-inverting input 115 and inverting input 116 of comparator 111, respectively. Comparator 111 finally evaluates voltages at both inputs to
15 set an output signal O_0 at an output terminal 117.

The same process for second, third, and fourth groups works as well as the above for the first group, that allows comparators 118-119 to provide output signals O_1 - O_3 at
output terminal 118-120, respectively. Furthermore, memory
20 banks 92-94 operate in the same function as memory bank 91, as a result output signals O_4 - O_{15} are furnished. Accordingly, memory device 90, which has four memory banks, each bank including four groups, simultaneously provides
sixteen outputs.

25 Thus, a new and improved MRAM device has been fully disclosed which allocates memory banks on a substrate, each memory bank including bit lines and a reference line on which magnetic memory cells and reference memory cells are arrayed.
30 These cells have very thin layers. In generally, it is very hard to uniformly control the width of layers over the entire substrate in order for all the cells to have the same hysteresis characteristic curves. In this MRAM device, bit lines are placed on both sides of the reference line in each

memory bank. This feature provides a steady reading function because a target cell that is close to a reference cell is selected and activated, and both cells have substantially the same hysteresis characteristics.

CLAIMS

1. A magnetic random access memory array comprising:
a plurality of first line groups, each of the plurality
5 of the first line groups having a plurality of first lines
placed in parallel and being electrically conductive;
a plurality of second lines being perpendicular to the
plurality of first lines and electrically conductive;
10 a plurality of magnetic memory cells, one each placed
on each intersection of the plurality of first lines and the
plurality of second lines and being electrically coupled to
a first line at the intersection;
a reference line being parallel to the plurality of
first lines and electrically conductive; and
15 a plurality of reference magnetic memory cells, one
each placed on each intersection of the reference line and
the plurality of second lines, and electrically coupled to
the reference line;
wherein each magnetic memory cell and each reference
20 magnetic memory cell have magnetic layers separated by a
non-magnetic layer.

2. The magnetic random access memory array as claimed
in claim 1 further including a plurality of comparators,
25 each comparator having a first input, a second input, and an
output, the first input being coupled to the plurality of
first lines in each first line group and the second input
being coupled to the reference line.

30 3. The magnetic random access memory array as claimed
in claim 2 further including a line selector for
electrically connecting the first input to one of the
plurality of first lines in the each first line group.

4. The magnetic random access memory array as claimed in claim 1 further including a plurality of switches and a plurality of reference switches, each switch being connected to each magnetic memory cell which allows a current to flow in the each magnetic memory cell, and each reference switch being connected to each reference magnetic memory cell which allows a reference current to flow in the each reference magnetic memory cell.

10

5. The magnetic random access memory array as claimed in claim 1 further including a second line controller for activating one of the plurality of second lines.

6. A magnetic random access memory array comprising:
a semiconductor substrate on which the magnetic random
access memory array is formed;

5 reference magnetic memory cells placed on a reference
line being electrically conductive; and
memory banks, each memory bank including magnetic
memory cells and being symmetrically placed on both sides of
the reference line.

10 7. The magnetic random access memory array as claimed
in claim 6 wherein each of the reference magnetic memory
cells and each of the magnetic memory cells have magnetic
layers separated by a non-magnetic layer.

8. A magnetic random access memory device comprising:
a plurality of memory arrays, each memory array
including:

5 a plurality of memory banks, each memory bank
having a plurality of magnetic memory cells placed on
intersections of first lines and second lines perpendicular
to the first lines, first and second lines being
electrically conductive and each magnetic memory cell being
electrically coupled to a first line on each intersection,
10 and

a plurality of reference magnetic memory cells
placed on intersections of a reference line in parallel with
the second lines and the second lines, the reference line
being electrically conductive and each reference magnetic
15 memory cell being electrically coupled to the reference line
on each intersection;

a first controller coupled to the plurality of first
lines and the reference line for activating one of the
plurality of first lines and the reference line in each
20 memory bank;

a second controller coupled to the plurality of second
lines for activating one of the plurality of second lines;

a line selector for selecting the one of the plurality
of first lines in each memory bank; and

25 a plurality of comparators, each comparator having a
first input, a second input and an output, the first input
being coupled to the one of the plurality of first lines and
the second comparator being coupled to the reference line.

9. The magnetic random access memory device as claimed in claim 8 wherein the magnetic memory cell has a first magnetic layer, a second magnetic layer, and a non-magnetic layer sandwiched by the first and second magnetic layers, the first magnetic layer electrically connected to the first line.

10. The magnetic random access memory array as claimed in claim 9 further including a plurality of switches, each switch connected to each second line for electrically coupling the second layer of each magnetic memory to a common line.

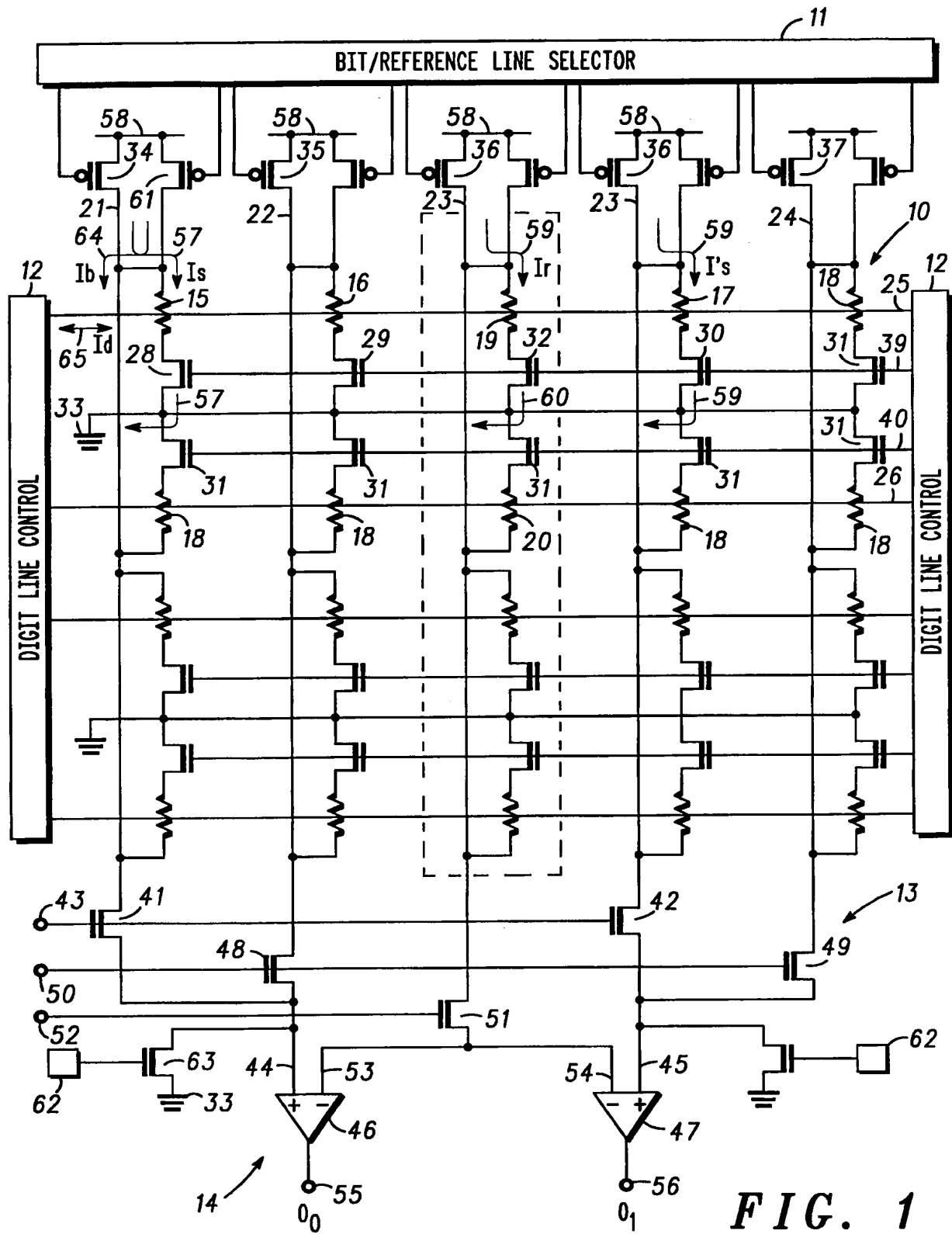


FIG. 1

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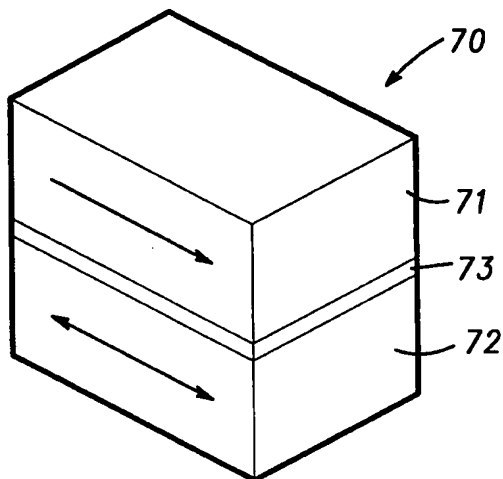


FIG. 2

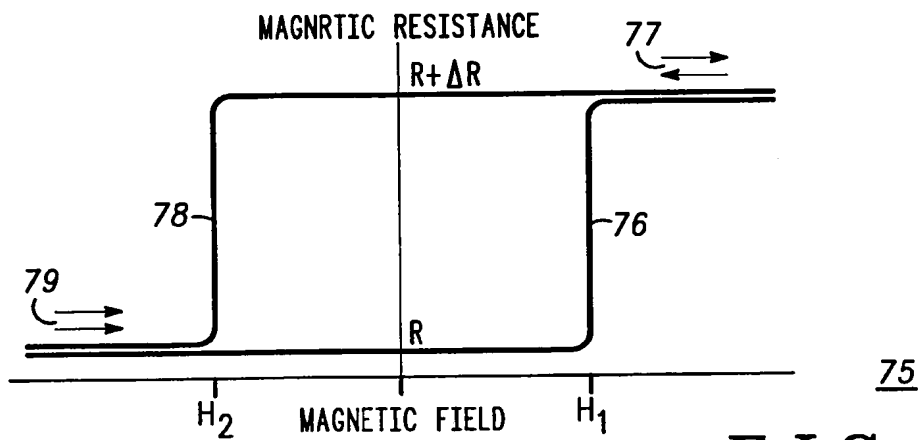


FIG. 3

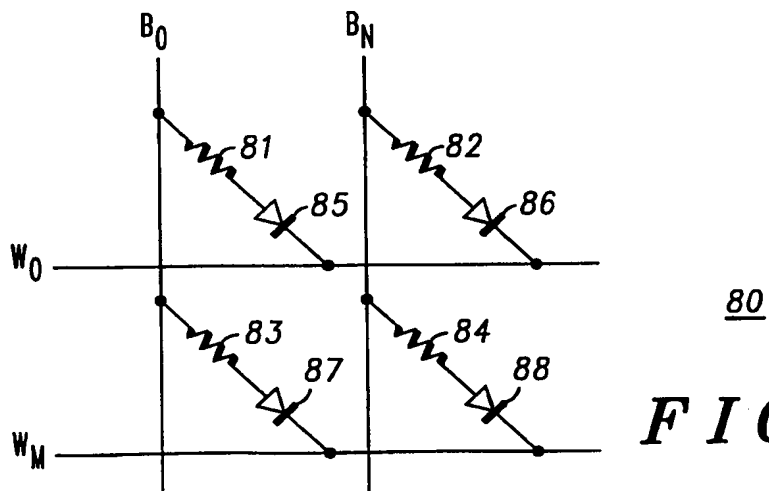


FIG. 4

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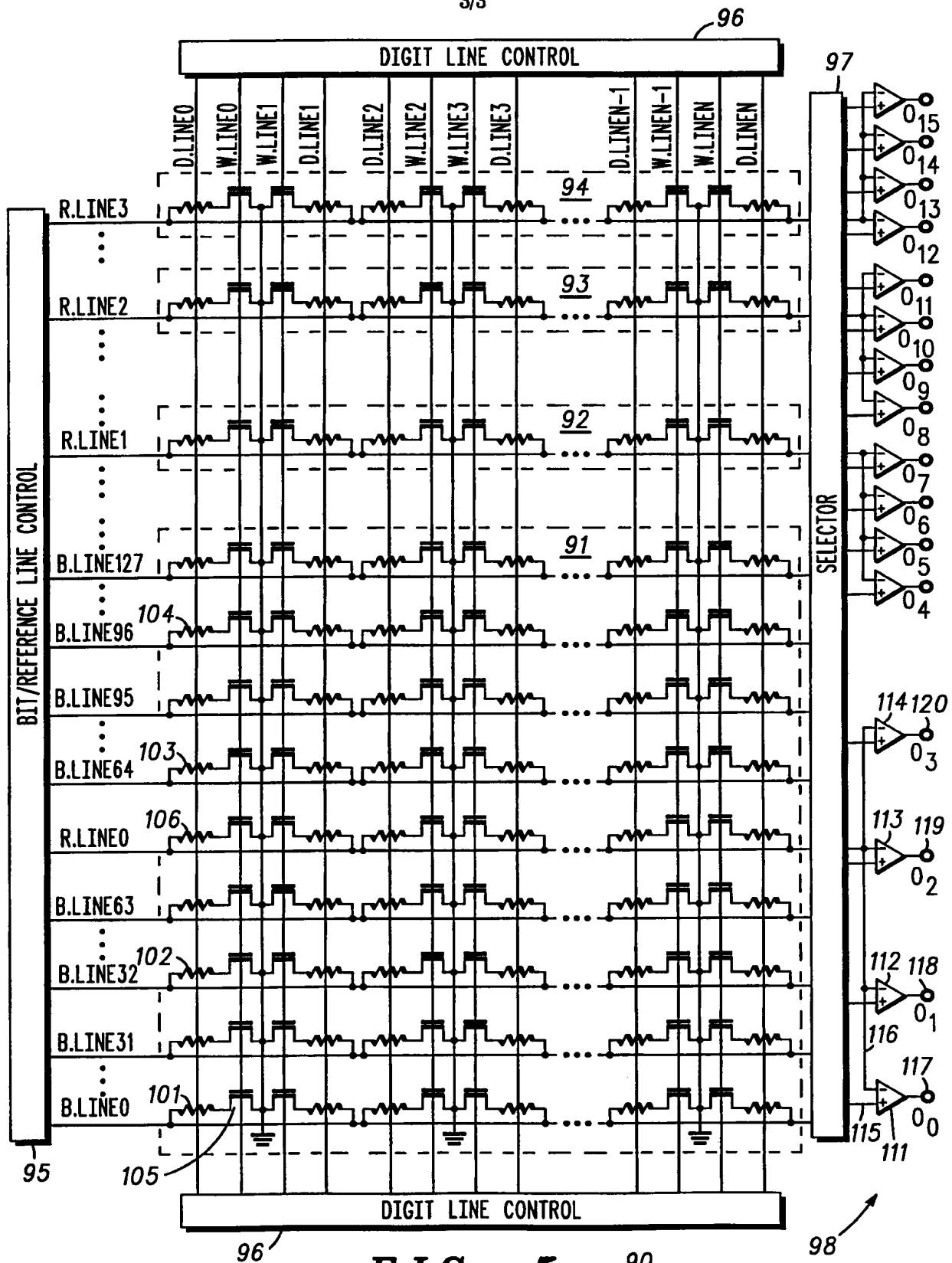


FIG. 5